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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Docket No: F0556

In re Appellant:

	Ming-Ren Lin	:	Art Unit:	2823
Serial No:	09/824,933	:	Examiner:	Khiem D. Nguyen
Filed:	April 03, 2001	:	Confirmation No.	1551

For: SCRIBE LANE FOR GETTERING OF CONTAMINANTS ON SOI WAFERS AND GETTERING METHOD

APPEAL BRIEF

VIA FACSIMILE
M/S Appeal Briefs - Patents
Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313

Dear Sir:

This Appeal Brief is submitted in the above-identified application in response to the final Office Action mailed 07 September, 2004. Appellants' Notice of Appeal was received in OIPE on October 11, 2004. Accordingly, Appellants' Appeal Brief is timely filed, with no extension of time.

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For: SCRIBE LANE FOR GETTERING OF CONTAMINANTS ON SOI WAFERS AND GETTERING METHOD

APPEAL BRIEF

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313

Dear Sir:

This Appeal Brief is submitted in the above-identified application in response to the final Office Action mailed September 07, 2004. Appellants' Notice of Appeal was received in OIPE on October 11, 2004.

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is Advanced Micro Devices, Inc., One AMD Place, Sunnyvale, California 94088.

II. RELATED APPEALS AND INTERFERENCES

Appellants are aware of no related pending appeals or interferences.

III. STATUS OF CLAIMS

Claims 1-15 and 21-25 are presently pending in the Application. Claims 1, 2, 5-9, 11-15 and 21-24 have been allowed and claims 3, 4, 10 and 25 stand finally rejected and

are the subject of the present Appeal. The Appendix contains a copy of all of claims 1-15 and 21-25.

IV. STATUS OF AMENDMENT

An amendment under 37 C.F.R. 1.116(a) was filed in this application, and the Examiner issued an Advisory Action. Thus, at the present time, there is no amendment pending.

V. SUMMARY OF CLAIMED INVENTION

Appellants' invention, in one embodiment as described in claim 1, relates to a method of manufacturing a semiconductor device on a silicon-on-insulator wafer 100 (p. 7, line 19 to p. 8, line 17) including a silicon active layer 102 having at least two die pads 104 formed thereon, the at least two die pads 104 separated by at least one scribe lane 106, comprising the steps of:

forming at least one cavity 120 through the silicon active layer 102 in the at least one scribe lane (S1001, Fig. 10; p. 8, line 18 to p. 10, line 25 and Figs. 2-9 as referred to therein);

forming at least one gettering plug 108 in each said cavity, each said gettering plug 108 comprising doped fill material containing a plurality of gettering sites (S1002, Fig. 10, and p. 11, lines 3-11 or S1003 and S1004, Fig. 10, and p. 11, lines 12-23); and

subjecting the wafer 100 to conditions to getter at least one impurity into the plurality of gettering sites (S1005, Fig. 10 and p. 14, line 28 to p. 16, line 17).

As set forth in claim 3 and in the specification, for example, at page 13, lines 24-26, the dopant recited in claim 1 may be one or more selected from phosphorus, arsenic, antimony, bismuth, boron, aluminum, gallium, indium, helium, neon, argon, krypton, xenon and germanium, when the dopant has been implanted.

Appellants' invention, in one embodiment as described in claim 9, relates to a method of gettering impurities on a silicon-on-insulator wafer 100 (p. 7, line 19 to p. 8, line

17) including a silicon active layer 102 having at least two die pads 104 formed thereon, the at least two die pads 104 separated by at least one scribe lane 106, comprising the steps of:

forming at least one cavity 120 through the silicon active layer 102 in the at least one scribe lane (S1001, Fig. 10; p. 8, line 18 to p. 10, line 25 and Figs. 2-9 as referred to therein);

filling the cavity 120 with a fill material (S1002 or S1003, Fig. 10, and p. 10, line 26 to p. 11, line 2);

adding at least one dopant to the fill material to form at least one gettering plug 108 including a plurality of gettering sites (S1002, Fig. 10, and p. 11, lines 3-11 or S1003 and S1004, Fig. 10, and p. 11, lines 12-23); and

subjecting the wafer 100 to conditions to getter at least one impurity into the plurality of gettering sites (S1005, Fig. 10 and p. 14, line 28 to p. 16, line 17).

As set forth in claim 10 and in the specification, for example, at page 13, lines 24-26, the dopant recited in claim 9 may be one or more selected from phosphorus, arsenic, antimony, bismuth, boron, aluminum, gallium, indium, helium, neon, argon, krypton, xenon and germanium. As set forth in claim 12, the fill material may be polysilicon and the dopant may be added by one of codeposition and implantation.

Appellants' invention, in one embodiment as described in claim 21, relates to a method of gettering impurities on a silicon-on-insulator wafer 100 including a silicon active layer 102, a buried oxide layer 110 and a silicon substrate 112, the silicon active layer 102 having at least two die pads 104 formed thereon, the at least two die pads 104 separated by at least one scribe lane 106, comprising the steps of:

forming a plurality of cavities 120 through the silicon active layer 102 and the buried oxide layer 110 to the silicon substrate 112 in the at least one scribe lane 106 (p. 8, line 18 to p. 10, line 25);

filling the cavities 120 with a fill material (S1003, Fig. 10, and p. 11, lines 12-14);

implanting at least one dopant into the fill material in the cavities 120 to form at least one gettering plug 108 including a plurality of gettering sites (S1004, Fig. 10, and p. 11, lines 14-16 and Fig. 8); and

subjecting the wafer 100 to conditions to getter at least one impurity into the plurality of gettering sites (S1005, Fig. 10 and p. 14, line 28 to p. 16, line 17).

As set forth in the specification, for example, at page 13, lines 24-26, the at least one dopant implanted in the implanting step may be one or more of phosphorus, arsenic, antimony, bismuth, boron, aluminum, gallium, indium, helium, neon, argon, krypton, xenon and germanium.

The present invention addresses the problem of gettering impurities from silicon-on-insulator wafers by providing gettering sites formed by adding dopants to materials in or near scribe lanes, thereby drawing impurities out of the wafer active areas into areas that will be inactive or removed from the finished wafers. By the addition of dopants to the fill material, the gettering capability of the fill material is increased due to the formation of additional gettering sites by the added dopants. As clearly defined in the claims and specification, the dopants may comprise a material which when added to the fill material, results in the formation of gettering sites.

VI. ISSUES ON APPEAL

The claims on appeal stand rejected based on the Examiner's objection to Appellant's claim terms. The issue in this appeal is:

APPELLANT'S USE OF THE TERM DOPANT AS DEFINED IN THE SPECIFICATION AND CLAIMS 3, 4, 10 and 25 IS NOT INDEFINITE AND NO PROPER, LEGAL BASIS FOR THE EXAMINER'S REJECTION OF THESE CLAIMS EXISTS.

VII. GROUPING OF CLAIMS

Claims 3, 4, 10 and 25 stand or fall together. Claims 1, 2, 5-9, 11-15 and 21-24 have been allowed and are not appealed, except to the extent the definition of the term

"dopant" as used in these claims is affected by the objection to the term "dopant" as defined in the specification and used in the claims under appeal.

VIII. ARGUMENT

A. Appellant Is Entitled to Act As His Own Lexicographer in Defining the Term "Dopant".

Claims 3, 4, 10 and 25 stand rejected based on the Examiner's refusal to accord Appellant's clear definition of the term "dopant" the full range of the definition as set forth in the specification. Claim 4 is rejected based only on its dependency on claim 3, so the following discussion refers only to claims 3, 10 and 25. In the final Office Action, claims 3, (4,) 10 and 25 were objected to, and finally rejected, based on the Examiner's contention that "'helium, neon, argon, krypton and xenon' are not considered as dopant materials in semiconductor devices." The Examiner "required" correction and omission of these terms, Appellant respectfully declined and continues to decline to do so. Appellant respectfully requests the Board to reverse the Examiner's rejection of claims 3, 10 and 25.

Applicant respectfully traverses the objection to the definition of the term "dopant" in claims 3, 10 and 25 and respectfully declines to amend the claims as requested. This "requirement" on the part of the Examiner is based on the apparent failure of the Examiner to understand and/or accord Applicant's clear and consistent use of the term given the scope of this term as disclosed in Applicant's specification and claims.

Claim language defines claim scope. *SRI Int'l v. Matsushita Elec. Corp.*, 775 F.2d 1107, 1121, 227 USPQ 577, 586 (Fed. Cir. 1985) (en banc). As a general rule, claim language carries the ordinary meaning of the words in their normal usage in the field of invention. *Toro Co. v. White Consol. Indus.*, 199 F.3d 1295, 1299, 53 USPQ2d 1065, 1067(Fed. Cir. 1999). Nevertheless, the inventor may act as his own lexicographer and use the specification to supply implicitly or explicitly new meanings for terms. *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979-80, 34 USPQ2d 1321, 1330 (Fed. Cir. 1995) (*en banc*),citing *In re Vogel*, 422 F.2d 438, 441, 164 USPQ 619, 621 (CCPA 1970)

("Occasionally the disclosure will serve as a dictionary for terms appearing in the claims, and in such instances the disclosure may be used in interpreting the coverage of the claim."). Even when guidance is not provided in explicit definitional format, "the specification may define claim terms 'by implication' such that the meaning may be 'found in or ascertained by a reading of the patent documents.'" *Bell Atl. Network Servs., Inc. v. Covad Communications Group, Inc.*, 262 F.2d 1258, 1268, 59 USPQ2D 1865, 1870-71 (Fed. Cir. 2001). That is, a claim term may be clearly redefined without an explicit statement of redefinition in the specification. *Id.* at 1870.

One looks to the specification "to ascertain the meaning of a claim term as it is used by the inventor in the context of the entirety of his invention." *Comark Communications v. Harris Corp.*, 156 F.3d 1182, 1187, 48 USPQ2d 1001, 1005 (Fed. Cir. 1998). The term "dopant", as used throughout the specification and claims, refers to a material added to the trench fill material to create a plurality of gettering sites.

While it may be true that, *usually*, in the semiconductor art, a dopant is added to a material such as silicon to change its electrical properties, it is also easily understood by those of ordinary skill in the semiconductor art that, more generally, a dopant is added to alter or change one or more property of the material to which the dopant is added. This slightly broader definition of the term "dopant" is that consistently used by Appellant in the specification and claims of this application. See, e.g., *Hoechst Celanese Corp. v. B.P. Chems. Ltd.*, 78 F.3d 1575, 1578, 38 USPQ2d 1126, 1129 (Fed. Cir. 1996) ("A technical term used in a patent document is interpreted as having the meaning that it would be given by persons experienced in the field of the invention, *unless it is apparent* from the patent and the prosecution history *that the inventor used the term with a different meaning.*") (Emphasis added.)

Therefore, Appellant has clearly exercised his right to act as his own lexicographer in the present application, in using the term "dopant" to refer to materials added to a substrate material to create gettering sites, which is only slightly broader than that in which

the term "dopant" is more often used. It is a meaning that is certainly not so different as to justify the Examiner's final rejection of Appellant's claims 3, 10 and 25.

Applicant respectfully submits that the Examiner is incorrectly taking the position that the term "dopant" must be given its "usual" usage in the semiconductor field, that is, as a material added to change the electrical conductivity of a material such as silicon. The Examiner's position is in contravention to the clear definition and usage in Applicant's specification. The Examiner's position is in contravention to the clearly enunciated law. In the present application, Applicant has acted as his own lexicographer and has used the specification to supply a broader meaning for the term "dopant" than that contended by the Examiner. This is entirely proper and accords with the law as enunciated by both the Federal Circuit and the CCPA, as set forth above.

B. Appellant's Definition of the Term "Dopant" Is Clearly Set Forth in the Specification.

It is clear from the specification that Appellant has attributed a meaning to the term "dopant" that is slightly broader than the ordinary and customary meaning in the semiconductor art, in which the term more often refers to a material or impurity added to silicon to alter its electrical characteristics. The written description shows that the Appellant used the term "dopant" to describe a material or impurity added to another material, in this case the material used to fill the trenches, to alter its gettering characteristics. In doing so, the Appellant has acted as his own lexicographer, and the Appellant's definition trumps the ordinary and customary meaning that otherwise would have attached. *3M Innovative Props. Co. v. Avery Dennison Corp.*, 350 F.3d 1365, 1374, 69 USPQ2d 1050, 1054 (Fed. Cir. 2003). "The specification acts as a dictionary when it expressly defines terms used in the claims or when it defines terms by implication." *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582, 39 USPQ2d 1573, 1577 (Fed. Cir. 1996). In this application, the Appellant has clearly defined this term.

Appellant's claim 1 recites a step of "forming at least one gettering plug in each said cavity, each said gettering plug comprising doped fill material containing a plurality of gettering sites". Appellant's claim 9 recites a step of "adding at least one dopant to the fill material to form at least one gettering plug including a plurality of gettering sites". Appellant's claim 21 recites a step of "implanting at least one dopant into the fill material in the cavities to form at least one gettering plug including a plurality of gettering sites". Thus, in each of Appellant's allowed independent claims, a "dopant" is added to the material forming the gettering plugs, thus to form a plurality of gettering sites.

Thus, Appellant has clearly exercised his right to act as his own lexicographer in the present application, in using the term "dopant" to refer to materials added to a substrate material to obtain desired, changed characteristics thereof, i.e., to create gettering sites in materials that either would not have gettering sites at all or that have enhanced gettering capability due to the presence of the added dopants. Appellant has used the term "dopant" to describe an impurity added to another material (the trench fill material) to alter the gettering characteristics of the trench fill material. In the present application, the desired, changed characteristic is the ability of the doped material to act as a gettering plug. Rejected claims 3, 10 and 25 merely identify specific dopants which can be used for the purpose set forth in the independent claims.

Referring to an embodiment where the trench fill material is polysilicon, as disclosed in the specification from page 11, line 30 to page 12, line 3:

> As described below, including dopant ions in the polysilicon results in the formation of better gettering sites, into which gettered impurities not only migrate, but which also more effectively trap the impurities. Ordinary polysilicon, even stressed polysilicon, does not trap impurities as effectively as does the doped polysilicon of the present invention.

Thus, the property of trapping impurities in gettering sites is the desired physical property obtained by the dopants added to the plug fill material in the present invention. The dopant

is not added for the purpose of altering the electrical properties, contrary to the more narrow use of the term "dopant" advanced by the Examiner.

As set forth in the specification, for example, at page 6, lines 26-27:

> The gettering plug 108 may be formed of a suitable fill material, e.g., polysilicon, doped with at least one dopant to form a plurality of gettering sites.

Thus, the "dopant" is the material added to the fill material to form the gettering sites. As shown by this sentence, the dopant is not added to the fill material for the purpose of changing the electrical conductivity of the fill material. Rather, the dopant is added to form the plurality of gettering sites. This is stated again, for example, at page 12, lines 16-22:

> The dopants which may be co-deposited with the polysilicon, i.e., by LPCVD, include phosphorus, arsenic, antimony, bismuth, boron, aluminum, gallium, indium, and germanium. These dopants may be co-deposited by providing a source of such dopants together with a source of silicon for the polysilicon. For example, when the dopant is phosphorus, a material such as phosphine (PH_3) may be provided to the deposition apparatus along with a source of silicon such as silane (SiH_4). Any suitable source of such dopants known in the art may be employed.

In another embodiment of the presently disclosed and claimed invention, the dopant is implanted into the previously-filled trench to form a gettering plug containing a plurality of gettering sites. This is defined, for example, at page 12, lines 23-27:

> In an alternative cavity filling step, in a first deposition step, shown as step S1003 in Fig. 10, the cavity 120A is filled with a fill material such as polysilicon to form the non-doped fill material 124. In a second step, shown as step S1004 in Fig. 10, dopant ions are implanted into the fill material 124, thereby to form the doped fill material 122, including a plurality of gettering sites in the nascent gettering plug.

This definition is followed at page 13, lines 24-26, by a list of dopants which may be implanted:

> The at least one dopant implanted in the step S1004 may be one or more of phosphorus, arsenic, antimony, bismuth, boron, aluminum, gallium, indium, helium, neon, argon, krypton, xenon and germanium.

The dopant and its function in the present invention is further defined at page 14, lines 18-20:

> Whether the dopant is formed by co-deposition with the fill material, or is implanted subsequent to deposition of the fill material, the amount of the dopant should be sufficient to obtain the number and distribution of gettering sites desired.

Based on the disclosure of the specification as a whole, as exemplified by the foregoing, it is clear and beyond cavil that Appellant's use of the term "dopant" has been fully and clearly defined in the specification and that it must be interpreted to include at least all of the dopant materials set forth in both the specification and in claims 3, 10 and 25.

Appellant respectfully submits that for at least the foregoing reasons, the claim term "dopant" is clear and in accordance with 35 U.S.C. 112, first and second paragraphs and, as such, the term "dopant" as used in the claims are defined in the specification such that a person of ordinary skill in the art would easily understand the scope of this term to include all of the elements set forth in claims 3, 10 and 25 and so the claims are not objectionable and should not have been rejected. Accordingly, Appellant respectfully requests the Board to reverse the rejection of claims 3, 4, 10 and 25.

C. Appellant's Definition of the Term "Dopant" Is Consistent, Can Be Readily Ascertained from the Specification and Does Not Deprive the Claims of Clarity.

An applicant is allowed to be his own lexicographer, unless the term chosen by the applicant so deprives the claim of clarity that there is no means by which the scope of the claim may be ascertained from the language used. *Johnson Worldwide Assocs., Inc. v. Zebco Corp.*, 175 F.3d 985, 990, 50 USPQ2d 1607, 1610 (Fed. Cir. 1999). Appellant's use of the term dopant cannot be considered or construed as so depriving the claim of clarity.

On the contrary, the scope of the claim is easily understood. Most often, the specification "is the single best guide to the meaning of a disputed term." *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582, 39 USPQ2d 1573 (Fed. Cir. 1996). Appellant has consistently used the term "dopant" throughout the specification and claims to refer to a material or impurity added to another material, e.g., the trench fill material, to alter its gettering characteristics.

The Examiner contends that the term "dopant" can refer only to an impurity added to another material such as silicon to alter its electrical characteristics. This is an incorrect, clearly erroneous and unreasonably narrow and limiting definition of this term. Contrary to the Examiner's contention, the term "dopant" is widely known in the semiconductor, materials and chemical arts to refer to an impurity added to another material to alter some characteristic from that which the material would have in the absence of the dopant. It is known in the art that dopants are added to alter not only electrical characteristics, but also to alter chemical characteristics such as etchability, thermal characteristics such as melting point, optical characteristics such as color, refractive index and light scattering in liquid crystals, and physical characteristics such as strength. In the following, Appellant presents only a few of the many uses of the term "dopant" known from the U.S. patent literature, all of which refer to an impurity added to another material to alter one or more characteristic from that which the material would have in the absence of the dopant.

U.S. Patent No. 4,066,569 discloses metallocene **dopants for liquid crystal materials to address the scattering characteristic** problems known in the art. In the background section of this patent, charge-transfer complexes as **dopants for liquid crystal materials added to lower the threshold voltage** are also disclosed.

U.S. Patent No. 4,795,685 discloses the use of a **dopant for a sodium aluminum chloride molten salt electrolyte** used to lower the melting point of the electrolyte.

U.S. Patent No. 4,859,017 discloses the use of a **dopant for a waveguide to alter the optical properties** thereof, in addition or alternative to **conventional dopants added to modify the refractive index** thereof.

U.S. Patent No. 5,094,693 discloses the use of a **dopant for zinc oxide pigments** to alter the apparent color to increase the blue absorption and to make it appear whiter.

U.S. Patent No. 5,366,939 discloses the use of **first and second metal dopants for a gradient index optical element to alter the refractive index** of the lens material.

U.S. Patent No. 5,548,154 discloses the use of **dopants selectively added to semiconductor materials to alter the etchability** of the doped materials relative to non-doped portions of the materials. As disclosed therein, an n-type doped epitaxial layer is anodized faster than p-type doped substrate on which the n-type doped epitaxial layer was deposited.

U.S. Patent No. 5,609,926 discloses a **dopant added to diamond to alter its optical or electrical properties.**

U.S. Patent No. 5,817,571 discloses a **dopant added to a glass layer to reduce the microloading effect** when an interlevel dielectric is planarized.

U.S. Patent No. 5,841,926 discloses a **dopant added to a silica glass to render it more sensitive to radiation** for preparation of a planar waveguide.

U.S. Patent No. 5,928,959 discloses a **dopant added to silicate glass to lower the melting point** of the glass to allow reflow after the glass is deposited.

U.S. Patent No. 6,059,879 discloses a **dopant added to the outer periphery of a semiconductor wafer to enhance strength** of the wafer to alleviate slippage with monocrystalline lattices of the wafer.

U.S. Patent No. 6,348,740 discloses **dopants added to solder bumps in a flip-chip package** to change the melting characteristics of the solder bumps and thereby eliminate gaps between the bumps on a die and the corresponding bonding pads.

Appellant respectfully submits that the foregoing sampling demonstrates a variety of "dopant" materials known and used by those of ordinary skill in the art, for many purposes other than the unduly limited purpose contended by the Examiner. The foregoing proves, from the patent literature itself, that Appellant's use of the term "dopant" to include the noble gas atoms is not consistent with a broader, more common definition of the term

"dopant". Appellant respectfully submits that the foregoing shows that persons of ordinary skill in the art would readily recognize the slightly broader definition of "dopant" as defined and used by Appellant in the present specification and claims.

For this additional reason, Appellant respectfully requests the Board to reverse the Examiner's rejection of Appellant's claims 3, 4, 10 and 25.

D. Appellant's Use of the Term "Dopant" Complies with 35 U.S.C. §112, First and Second Paragraphs and with 37 CFR 1.75(d)(1).

Although the claims are rejected based on the Examiner's "objection" to the claims, and there is no statutory basis for the rejection, Appellant respectfully submits that the claims fully comply with 35 U.S.C. §112, first and second paragraphs. The full scope of the claims is adequately disclosed, is enabled and is not indefinite.

Furthermore, the claims fully comport with 37 CFR 1.75(d)(1), which reads as follows:

> (d)(1) The claim or claims must conform to the invention as set forth in the remainder of the specification and the terms and phrases used in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description.

As shown above, the term "dopant" as used in the claims finds both clear support and antecedent basis in the description, so that the meaning of the term "dopant" in the claims is easily ascertainable by reference to the description in the specification.

Because Appellant has defined and used the term "dopant" to encompass at least all of the elements specifically set forth in claims 3, 10 and 25, Appellant has fully complied with the Patent Statute and the Rules of Practice, as well as with the law as set forth by the Federal Circuit.

Accordingly, Appellant respectfully submits that the Examiner's "objection" to Appellant's use of this term and consequent final rejection of Appellant's claims is

clearly improper and should be reversed by the Board. Appellant requests the Board to reverse the rejection of claims 3, 4, 10 and 25 in the September 7, 2004 Office Action.

IX. CONCLUSION

For all these reasons, the rejection of Appellants' claims 3, 4, 10 and 25 based on the Examiner's objection to Applicant's clearly defined term "dopant" in the presently pending claims and specification should be reversed because Appellant has acted as his own lexicographer in defining and using the term in the specification and claims. Appellant respectfully requests reversal of the Examiner's rejections of Appellant's claimed invention of claims 3, 4, 10 and 25 based on this objection. Appellant respectfully submits that all of the pending claims are in condition for allowance, and respectfully request notice to such effect from the Examiner and/or the Board.

In the event issues remain in the prosecution of this application, Appellant requests that the Examiner telephone the undersigned attorney. **The Commissioner is expressly authorized to charge the 37 CFR 41.20(b)(2) fee for filing an Appeal Brief, $340.00, to the below deposit account.** If any additional fees are required for the filing of this paper, the Commissioner is authorized to charge those fees to Deposit Account #18-0988, Docket No. F0556, AMDSP0448US.

Respectfully submitted,
RENNER, OTTO, BOISSELLE & SKLAR

Date: October 22, 2004

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APPENDIX:

CLAIMS ON APPEAL

1. A method of manufacturing a semiconductor device on a silicon-on-insulator wafer including a silicon active layer having at least two die pads formed thereon, the at least two die pads separated by at least one scribe lane, comprising the steps of:

forming at least one cavity through the silicon active layer in the at least one scribe lane;

forming at least one gettering plug in each said cavity, each said gettering plug comprising doped fill material containing a plurality of gettering sites; and

subjecting the wafer to conditions to getter at least one impurity into the plurality of gettering sites.

2. The method of claim 1, wherein the doped fill material is polysilicon formed by LPCVD deposition of the polysilicon and a dopant in the cavity.

3. The method of claim 2, wherein the dopant is one or more selected from phosphorus, arsenic, antimony, bismuth, boron, aluminum, gallium, indium, helium, neon, argon, krypton, xenon and germanium.

4. The method of claim 3, wherein the dopant is phosphorus.

5. The method of claim 1, wherein the step of forming at least one cavity further comprises forming a sidewall liner in the cavity.

6. The method of claim 1, wherein the gettering plug extends down through the silicon active layer, and contacts a dielectric insulation layer on the wafer.

7. The method of claim 1, wherein the gettering plug extends down through both a silicon active layer and a dielectric insulation layer on the wafer.

8. The method of claim 7, wherein in the gettering step gettered impurities migrate into a silicon substrate layer below the dielectric insulation layer.

9. A method of gettering impurities on a silicon-on-insulator wafer including a silicon active layer having at least two die pads formed thereon, the at least two die pads separated by at least one scribe lane, comprising the steps of:

forming at least one cavity through the silicon active layer in the at least one scribe lane;

filling the cavity with a fill material;

adding at least one dopant to the fill material to form at least one gettering plug including a plurality of gettering sites; and

subjecting the wafer to conditions to getter at least one impurity into the plurality of gettering sites.

10. The method of claim 9, wherein the dopant is one or more selected from phosphorus, arsenic, antimony, bismuth, boron, aluminum, gallium, indium, helium, neon, argon, krypton, xenon and germanium.

11. The method of claim 9, wherein the step of forming at least one cavity further comprises forming a sidewall liner in the cavity.

12. The method of claim 9, wherein the fill material is polysilicon, and the dopant is added by one of codeposition and implantation.

13. The method of claim 9, wherein the gettering plug extends through the silicon active layer, and contacts a dielectric insulation layer on the wafer.

14. The method of claim 9, wherein the gettering plug extends through both the silicon active layer and a dielectric insulation layer on the wafer.

15. The method of claim 14, wherein in the gettering step gettered impurities move into a silicon substrate layer below the dielectric insulation layer.

21. A method of gettering impurities on a silicon-on-insulator wafer including a silicon active layer, buried oxide layer and a silicon substrate, the silicon active layer having at least two die pads formed thereon, the at least two die pads separated by at least one scribe lane, comprising the steps of:

forming a plurality of cavities through the silicon active layer and the buried oxide layer to the silicon substrate in the at least one scribe lane;

filling the cavities with a fill material;

implanting at least one dopant into the fill material in the cavities to form at least one gettering plug including a plurality of gettering sites; and

subjecting the wafer to conditions to getter at least one impurity into the plurality of gettering sites.

22. The method of claim 21, wherein in the gettering step, gettered impurities move into the silicon substrate.

23. The method of claim 21, wherein the wafer comprises a plurality of adjacent die pads and a single scribe lane separates each die pad from the adjacent die pads.

24. The method of claim 23, wherein the scribe lane comprises a single row of gettering plugs, a pair of parallel rows of gettering plugs or a pair of parallel gettering trenches.

25. The method of claim 21, wherein the dopant is one or more selected from phosphorus, arsenic, antimony, bismuth, boron, aluminum, gallium, indium, helium, neon, argon, krypton, xenon and germanium.